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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/737,638	12/14/2000	F. Scott Johnson	TI-23703.1	2828

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EXAMINER
HA, NATHAN W

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/737,638	JOHNSON, F. SCOTT	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Cancellation of claims 13 and 15 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chin et al. (US. 4,992,848, previously cited, hereinafter, Chin) and in view of Brighton (US 4,839,305, previously cited.) and Park (US 2001/0048134, newly cited.)

In regard to claim 14, Chin et al. discloses, in fig. 9, a method of forming an emitter contact for a bipolar junction transistor comprising steps of:

providing a silicon substrate 101 having a collector region 102, a base region 115 within collector region 102, and an emitter region 114 disposed within base region 115;

forming a base polysilicon layer 111 on the surface of silicon substrate 101 in contact with the base region 115, and defining an aperture with a sidewall (not numbered) exposing the base and emitter regions of the silicon substrate;

forming the aperture through the layers;

forming a spacer 109 extending upwardly from the silicon substrate and to cover the sidewalls, the spacers covering the base region and partially covering emitter region;

forming an emitter electrode 105 positioned within the aperture in engagement with emitter region, the spacer, and the substrate.

depositing a layer of emitter polysilicon 110 onto the substrate and the aperture. This limitation can be found in Chin's col. 3, lines 52-55; and

etching back the layer of emitter polysilicon, see figs. 4-5.

Chin et al. as describe above fails to disclose the method of forming the oxide layer as depositing an oxide layer onto the base polysilicon. It should be noted that deposition method is widely used in the semiconductor manufacturing to improving the device structure and eliminating unnecessary step in the process since deposition does not damage the lattice of the silicon structure; Therefore, the annealing process it not necessary.

Park, in fig. 3, teaches a method of making a bipolar transistor including a substrate 10, and further teaches depositing a layer of oxide 67 over the substrate.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the oxide layer by deposition method as taught by Park in Chin's in order to be able to obtain the advantages mentioned above.

4. Claims 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chin and Park as applied to claim 14 above, and further in view of Walczyk et al. (Tailoring Interface Oxide for Polysilicon..., IEEE, 1992, pp. 84-87, previously cited.)

In regard to claim 16, the combination of Chin and Park discloses all of the claimed limitations as mentioned above, but does not expressly mention the use of in situ and rapid thermal annealing in the process of making the device. It should be noted that the method of using "in situ" and annealing is well known and have being used widely in the art of making semiconductor devices since in situ can be used to producing a minimum interfacial oxide known as "Oxide Free process", and Rapid thermal annealing process can be used to avoid damaging the surface of the device. For example, Walczyk et al. evidently teaches these processes in his article of how to make an efficient semiconductor device; see page 84 col. 2 last paragraph and page 85, col. 2, first paragraph.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the processes as taught by Walczyk et al. in Chin in order to take advantages of these processes to improving device characteristics since in situ process can be used to producing a minimum interfacial oxide known as "Oxide Free process", and Rapid thermal annealing process can be used to avoid damaging the surface of the device.

Response to Arguments

5. Applicant's arguments with respect to claims 14 and 16 have been considered but are moot in view of the new ground(s) of rejection.

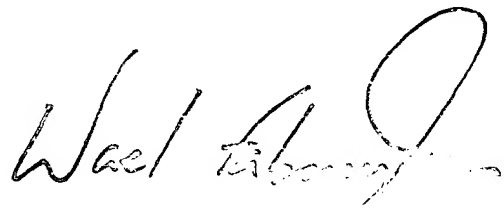
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (707) 305-3507. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 305-3431, or 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Nathan Ha
May 15, 2003



SUPERVISORY PRINCIPAL EXAMINER
TECHNOLOGY CENTER 2800